SUMMARY DOCUMENT WITH STATUS OF CLAIMS

IN THE CLAIMS:

Claim 1 (currently amended): A memory structure comprising:

a plurality of adjacent substrates stacked one on another;

a plurality of connectors connecting said substrates to one another; [and]

[at least one] a memory chip package mounted on each of said substrates[.]; and

a gap between a top of said memory chip package and a bottom of an adjacent substrate,

wherein said connectors have a size sufficient to form a [gap] space between said substrates, and

wherein said [gap] space is larger than a height of said memory chip package.

Claim 2 (original): The memory structure in claim 1, wherein said memory chip package comprises a pre-tested memory chip package that is tested for defects before being mounted on said substrates.

Claim 3 (original): The memory structure in claim 1, wherein said memory chip package and said substrates include identical electrical connections.

Claim 4 (original): The memory structure in claim 1, wherein each of said substrates has a plurality of said memory chip packages mounted thereon.

Claim 5 (original): The memory structure in claim 1, wherein said connectors comprises solder

balls.

Claim 6 (currently amended): The memory structure in claim 1, further comprising a thermal [connection] material between a top of said memory chip package and a bottom of an adjacent substrate[, such that said thermal connection fills said gap].

Claim 7 (original): The memory structure in claim 1, wherein said memory chip package comprises a chip having an array of memory elements mounted within a package.

Claim 8 (currently amended): A memory structure comprising:

a plurality of adjacent substrates stacked one on another;

a plurality of connectors connecting said substrates to one another; [and]

[at least one] a memory chip package mounted on each of said substrates[,]; and

a gap between a top of said memory chip package and a bottom of an adjacent substrate,

wherein said connectors have a size sufficient to form a [gap] space between said substrates,

wherein said [gap] space is larger than a height of said memory chip package, and

wherein each memory chip package includes only a single memory chip.

Claim 9 (original): The memory structure in claim 8, wherein said memory chip package comprises a pre-tested memory chip package that is tested for defects before being mounted on said substrates.

Claim 10 (original): The memory structure in claim 8, wherein said memory chip package and said substrates include identical electrical connections.

Claim 11 (original): The memory structure in claim 8, wherein each of said substrates has a plurality of said memory chip packages mounted thereon.

Claim 12 (original): The memory structure in claim 8, wherein said connectors comprise solder balls.

Claim 13 (currently amended): The memory structure in claim 8, further comprising a thermal [connection] material between a top of said memory chip package and a bottom of an adjacent substrate[, such that said thermal connection fills said gap and said memory chip package includes a single memory chip].

Claim 14 (original): The memory structure in claim 8, wherein said memory chip package comprises a chip having an array of memory elements mounted within a package.

Claims 15-20 (cancelled without prejudice or disclaimer)

Claim 21 (new): A vertically stacked memory module comprising:

a plurality of adjacent substrates stacked one on another;

a plurality of substrate spacers electrically connecting said substrates with one another;

a single memory chip package mounted on each of said substrates;

a plurality of package spacers connecting said memory chip package with said substrates; and

a gap between a top of said memory chip package and a bottom of an adjacent substrate,

wherein said memory chip package comprises a memory chip having an array of memory elements mounted within said package,

wherein said substrate spacers form a space between a top of said memory chip package and a bottom of said adjacent substrates, and

wherein said space is greater than a height of said memory chip package.

Claim 22 (new): The memory module in claim 21, wherein said memory chip package comprises a pre-tested memory chip package that is tested for defects before being mounted on said substrates.

Claim 23 (new): The memory module in claim 21, wherein said memory chip package and said substrates include identical electrical connections.

Claim 24 (new): The memory module in claim 21, wherein each of said substrates has a plurality of said memory chip packages mounted thereon.

Claim 25 (new): The memory module in claim 21, wherein said substrate spacers and said

package spacers comprise solder balls.

Claim 26 (new): The memory module in claim 21, further comprising thermal material between a top of said memory chip package and a bottom of an adjacent substrate.